LTC1596-1

Serial 16-Bit Multiplying DAC with Clear to Mid-Scale Input

July 1998

FEATURES

- Asynchronous Clear Input Clears DAC to Mid Scale
- **DNL and INL: 1LSB Max**
- **Low Glitch Impulse: 1nV-s Typ**
- Pin Compatible with Industry Standard 12-Bit DACs: LTC8143/LTC7543
- 4-Quadrant Multiplication
- Low Power Consumption
- Power-On Reset Clears DAC to Mid Scale
- Daisy-Chain Serial Output

APPLICATIONS

- Process Control and Industrial Automation
- Software Controlled Gain Adjustment
- Digitally Controlled Filter and Power Supplies
- Automatic Test Equipment

DESCRIPTION

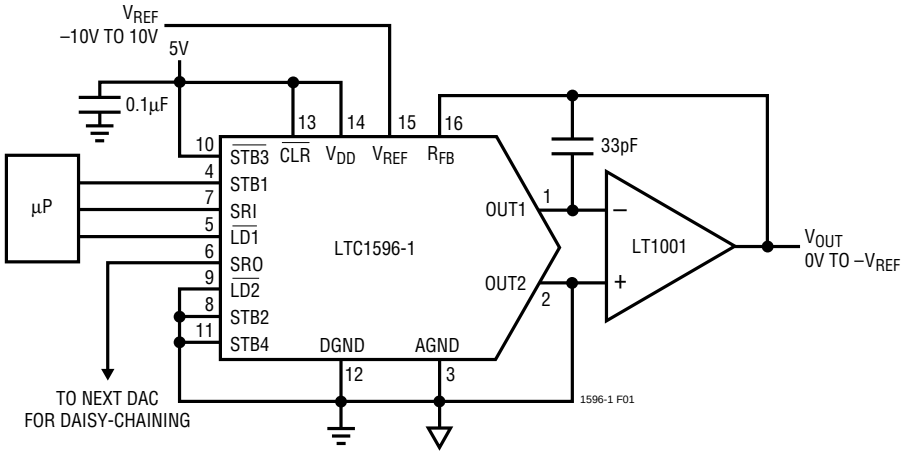
The LTC®1596-1 is a serial input, 16-bit multiplying current output DAC. The device is pin and hardware compatible with the 12-bit LTC8143/LTC7543 and comes in 16-pin PDIP and SO wide packages. It offers clear to mid scale for both the clear input and power-on reset. A related device, the LTC1596, is identical except it clears to zero scale.

The LTC1596-1 is specified over the industrial temperature range. Sensitivity of INL to op amp V_{OS} is reduced by five times compared to the industry standard 12-bit DACs, so most systems can be easily upgraded to true 16-bit resolution and linearity without requiring more precise op amps.

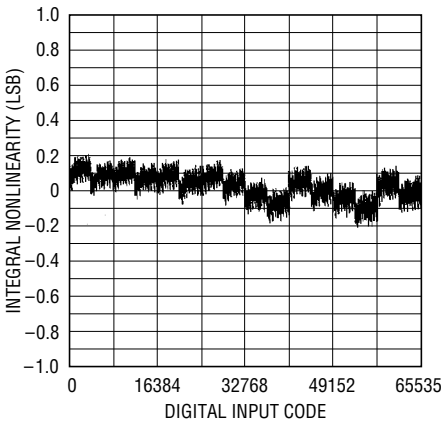
This DAC includes an internal deglitching circuit that reduces the glitch impulse by more than ten times to 1nV-s typ.

TYPICAL APPLICATION

Multiplying DAC Has Easy 3-Wire Serial Interface



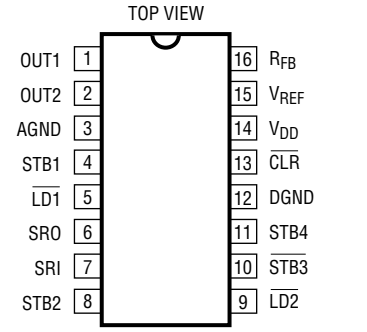
Integral Nonlinearity



ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... –0.5V to 7V
V_{DD} to DGND ..... –0.5V to 7V
AGND to DGND ..... V_{DD} + 0.5V
DGND to AGND ..... V_{DD} + 0.5V
V_{REF} to AGND, DGND ..... ±25V
R_{FB} to AGND, DGND ..... ±25V
Digital Inputs to DGND ..... –0.5V to V_{DD} + 0.5V
V_{OUT1}, V_{OUT2} to AGND ..... –0.5V to V_{DD} + 0.5V
Maximum Junction Temperature ..... 150°C
Operating Temperature Range
LTC1596-1C ..... 0°C to 70°C
LTC1596-1I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PDIP

SW PACKAGE
16-LEAD PLASTIC SO WIDE

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER
LTC1596-1ACN
LTC1596-1ACSW
LTC1596-1BCN
LTC1596-1BCSW
LTC1596-1CCN
LTC1596-1CCSW
LTC1596-1AIN
LTC1596-1AISW
LTC1596-1BIN
LTC1596-1BISW
LTC1596-1CIN
LTC1596-1CISW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1596-1A MIN	LTC1596-1A TYP	LTC1596-1A MAX	LTC1596-1B MIN	LTC1596-1B TYP	LTC1596-1B MAX	LTC1596-1C MIN	LTC1596-1C TYP	LTC1596-1C MAX	UNITS
Accuracy													
	Resolution		●	16			16			16			Bits
	Monotonicity		●	16			16			15			Bits
INL	Integral Nonlinearity	(Note 1) T_A = 25°C			±0.25	±1			±2			±4	LSB
		T_{MIN} to T_{MAX}	●		±0.35	±1			±2			±4	LSB
DNL	Differential Nonlinearity	T_A = 25°C			±0.2	±1			±1			±2	LSB
		T_{MIN} to T_{MAX}	●		±0.2	±1			±1			±2	LSB
GE	Gain Error	(Note 2) T_A = 25°C			2	±16			±16			±32	LSB
		T_{MIN} to T_{MAX}	●		3	±16			±32			±32	LSB

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Gain Temperature Coefficient	(Note 3) ΔGain/ΔTemperature	●		1	2	ppm/°C
$I_{LEAKAGE}$	OUT1 Leakage Current	(Note 4) T_A = 25°C				±3	nA
		T_{MIN} to T_{MAX}	●			±15	nA
	Zero-Scale Error	T_A = 25°C				±0.2	LSB
		T_{MIN} to T_{MAX}	●			±1	LSB
PSRR	Power Supply Rejection	V_{DD} = 5V ±10%	●		±1	±2	LSB/V
Reference Input							
R_{REF}	V_{REF} Input Resistance	(Note 5)	●	5	7	10	kΩ

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Performance							
	Output Current Settling Time	(Notes 6, 7)			1		µs
	Midscale Glitch Impulse	$C_{FEEDBACK}$ = 33pF			1		nV-s
	Digital-to-Analog Glitch Impulse	(Notes 6, 8)			1		nV-s
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sine Wave			1		mV_{P-P}
THD	Total Harmonic Distortion	(Note 9)			108		dB
	Output Noise Voltage Density	(Note 10) f = 1kHz			11		$nV/\sqrt{Hz}$
Analog Outputs							
C_{OUT1}	OUT1 Output Capacitance (Note 3)	DAC Register Loaded to All 1s DAC Register Loaded to All 0s	● ●		115 70	130 80	pF pF
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 3) V_{IN} = 0V	●			8	pF
V_{OH}	Digital Output High Voltage	I_{OH} = 200µA	●	4			V
V_{OL}	Digital Output Low Voltage	I_{OL} = –1.6mA	●			0.4	V
Timing Characteristics							
t_{DS1}	Serial Input to Strobe Setup Time	STB1 Used as the Strobe	●	30	5		ns
t_{DS2}		STB2 Used as the Strobe	●	20	–5		ns
t_{DS3}		$\overline{STB3}$ Used as the Strobe	●	25	0		ns
t_{DS4}		STB4 Used as the Strobe	●	20	–5		ns
t_{DH1}	Serial Input to Strobe Hold Time	STB1 Used as the Strobe	●	30	5		ns
t_{DH2}		STB2 Used as the Strobe	●	40	15		ns
t_{DH3}		$\overline{STB3}$ Used as the Strobe	●	35	10		ns
t_{DH4}		STB4 Used as the Strobe	●	40	15		ns
t_{SRI}	Serial Input Data Pulse Width		●	60			ns
t_{STB1} to t_{STB4}	Strobe Pulse Width	(Note 11)	●	60			ns
$t_{\overline{STB1}}$ to $t_{\overline{STB4}}$	$\overline{Strobe}$ Pulse Width	(Note 12)	●	60			ns
$t_{\overline{LD1}}$, $t_{\overline{LD2}}$	$\overline{LD1}$, $\overline{LD2}$ Pulse Width		●	60			ns
t_{ASB}	LSB Strobed into Input Register to Load DAC Register Time		●	0			ns
$t_{\overline{CLR}}$	Clear Pulse Width		●	100			ns
t_{PD1}	STB1 to SRO Propagation Delay	C_L = 50pF	●	30		150	ns
t_{PD}	STB2, $\overline{STB3}$, STB4 to SRO Propagation Delay	C_L = 50pF	●	30		200	ns

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V ±10%, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Supply Voltage		●	4.5	5	5.5	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{DD}	●		1.5	10	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: ±1LSB = ±0.0015% of full scale = ±15.3ppm of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: I_{OUT1} with DAC register loaded with all 0s.

Note 5: Typical temperature coefficient is 100ppm/°C.

Note 6: OUT1 load = 100Ω in parallel with 13pF.

Note 7: To 0.0015% for a full-scale change, measured from the falling edge of $\overline{LD1}$ or $\overline{LD2}$.

Note 8: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

Note 9: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s; op amp = LT1007.

Note 10: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K); R = resistance (Ω); T = temperature (°K); B = bandwidth (Hz).

Note 11: Minimum high time for STB1, STB2, STB4. Minimum low time for $\overline{STB3}$.

Note 12: Minimum low time for STB1, STB2, STB4. Minimum high time for $\overline{STB3}$.

PIN FUNCTIONS

OUT1 (Pin 1): True Current Output Pin. Tie to inverting input of current to voltage converter op amp.

OUT2 (Pin 2): Complement Current Output Pin. Tie to analog ground.

AGND (Pin 3): Analog Ground Pin.

STB1, STB2, $\overline{STB3}$, STB4 (Pins 4, 8, 10, 11): Serial Interface Clock Inputs. STB1, STB2 and STB4 are rising edge triggered inputs. $\overline{STB3}$ is a falling edge triggered input (see Truth Tables).

$\overline{LD1}$, $\overline{LD2}$ (Pins 5, 9): Serial Interface Load Control Inputs. When $\overline{LD1}$ and $\overline{LD2}$ are pulled low, data is loaded from the shift register into the DAC register, updating the DAC output (see Truth Tables).

SRO (Pin 6): The Output of the Shift Register. Becomes valid on the active edge of the serial clock.

SRI (Pin 7): The Serial Data Input. Data on the SRI pin is latched into the shift register on the active edge of the serial clock. Data is loaded MSB first.

DGND (Pin 12): Digital Ground Pin.

$\overline{CLR}$ (Pin 13): The Clear Pin for the DAC. Clears DAC to mid scale when pulled low. This pin should be tied to V_{DD} for normal operation.

V_{DD} (Pin 14): The Positive Supply Input. 4.5V ≤ V_{DD} ≤ 5.5V. Requires a bypass capacitor to ground.

V_{REF} (Pin 15): Reference Input.

R_{FB} (Pin 16): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp.

TRUTH TABLES

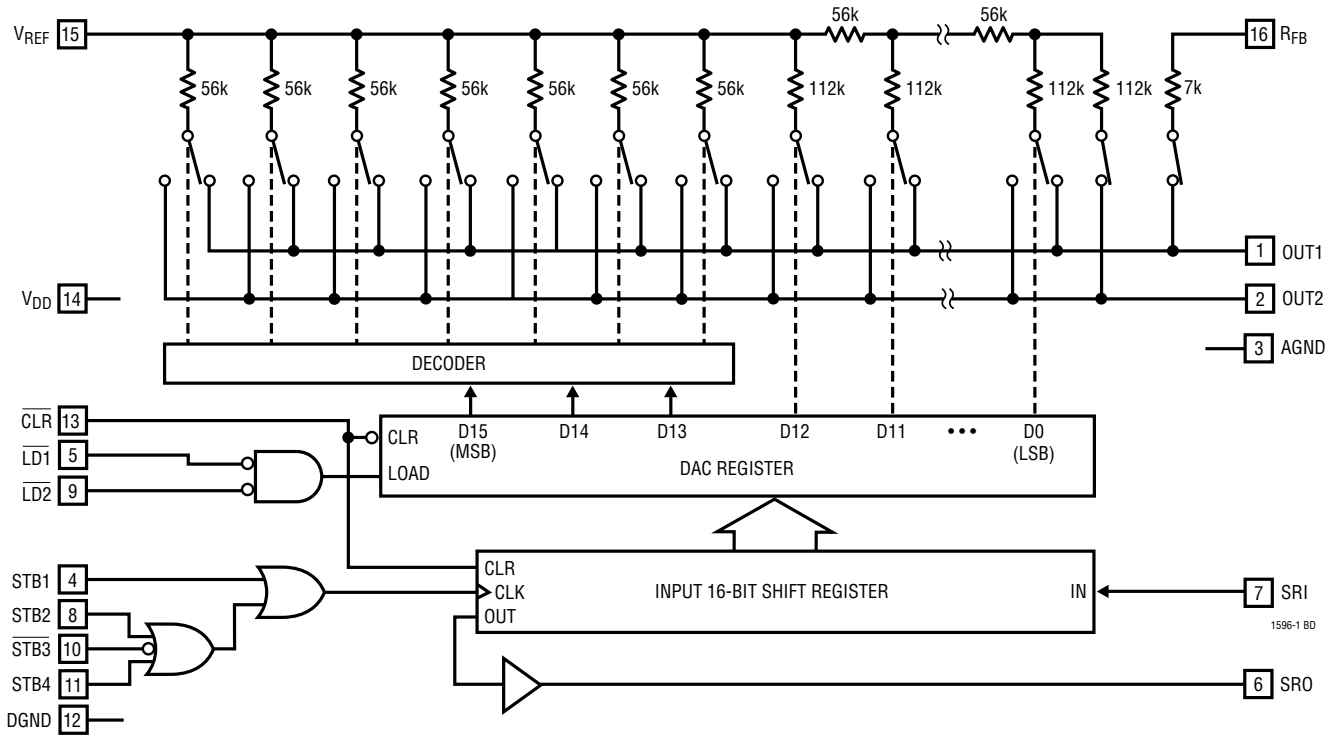
Table 1. LTC1596-1 Input Register

CONTROL INPUTS				
STB1	**STB2**	**$\overline{STB3}$**	**STB4**	**Input Register and SRO Operation**
↓	0	1	0	Serial Data Bit on SRI Loaded into Input Register, MSB First
0	↓	1	0	
0	0	↓	0	Data Bit or SRI Appears on SRO Pin After 16 Clocked Bits
0	0	1	↓	
1	X	X	X	No Input Register Operation
X	1	X	X	No SRO Operation
X	X	0	X	
X	X	X	1	

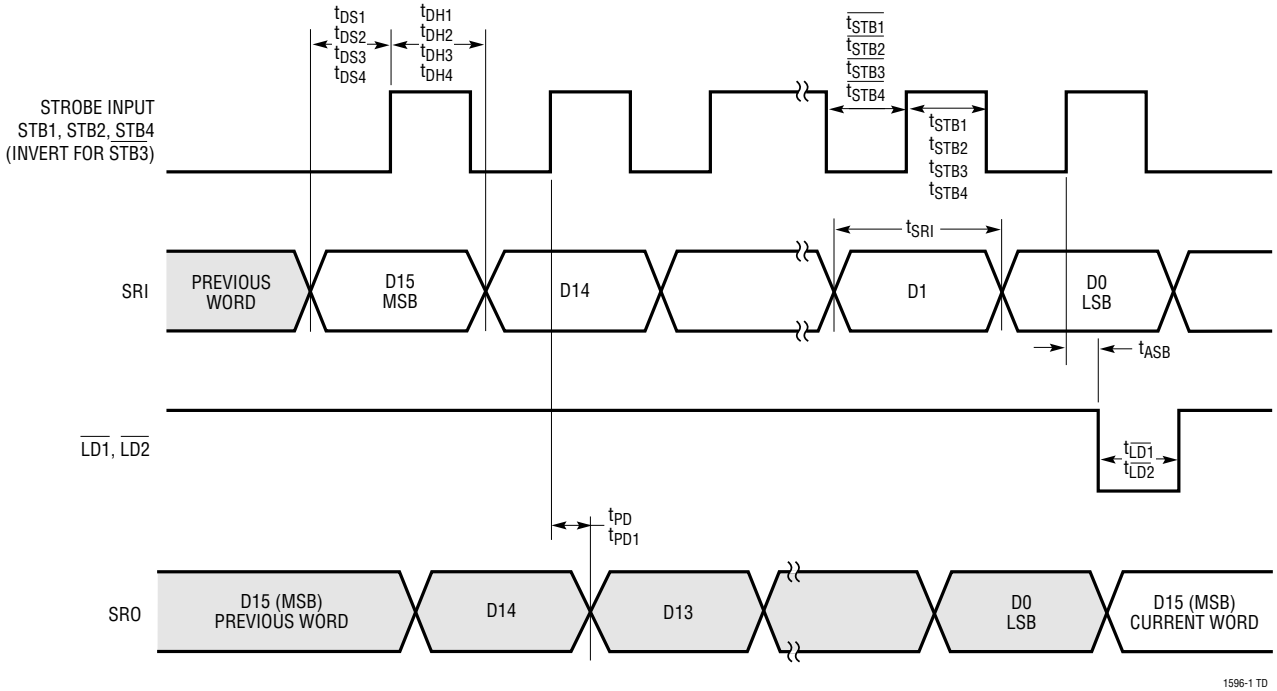
Table 2. LTC1596-1 DAC Register

CONTROL INPUTS			
$\overline{CLR}$	**$\overline{LD1}$**	**$\overline{LD2}$**	**DAC Register Operation**
0	X	X	Reset DAC Register and Input Register to 1000....000 (Mid Scale) (Asynchronous Operation)
1	1	X	No DAC Register Operation
1	X	1	
1	0	0	Load DAC Register with the Contents of Input Register

BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Description

The LTC1596-1 is a 16-bit multiplying DAC which has serial inputs and current outputs. It uses precision R/2R technology to provide exceptional linearity and stability. The device operates from a single 5V supply and provides ±10V reference input and voltage output ranges when used with an external op amp. This device has a proprietary deglitcher that reduces glitch energy to 1nV-s over a 0V to 10V output range.

Serial I/O

The LTC1596-1 has an SPI/MICROWIRE™ compatible serial port that accepts 16-bit serial words. Data is accepted MSB first and loaded with a load pin.

Data is shifted into the SRI data input on the rising edge of the strobe pin.

Four strobe pins are available STB1, STB2, $\overline{STB3}$ and STB4. STB1, STB2 and STB4 capture data on their rising edges. $\overline{STB3}$ captures data on its falling edge (see Truth Table 1).

The LTC1596-1 has two load pins, $\overline{LD1}$ and $\overline{LD2}$. To load data, both pins must be taken low. Normally one of the pins is grounded. An asynchronous clear input ($\overline{CLR}$) resets the LTC1596-1 to mid scale when pulled low (see Truth Table 2).

The LTC1596-1 also has a data output pin SRO that can be connected to the SRI input of another DAC to daisy-chain multiple DACs on one 3-wire interface (see the Timing Diagram).

2-Quadrant Multiplying Mode (V_{OUT} = 0V to $-V_{REF}$)

The LTC1596-1 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed –10V reference, the circuit shown gives a precision unipolar 0V to 10V output swing.

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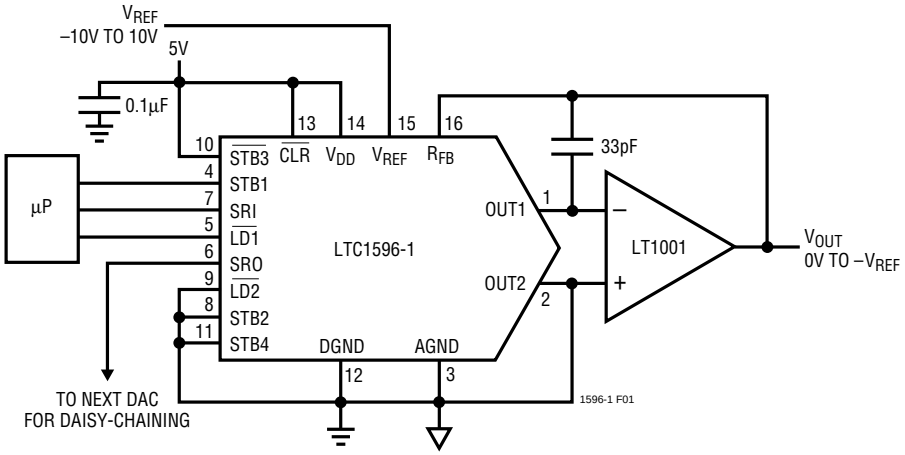


Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT V_{OUT}
MSB LSB	
1111 1111 1111 1111	$-V_{REF}$ (65,535/65,536)
1000 0000 0000 0000	$-V_{REF}$ (32,768/65,536) = $-V_{REF}/2$
0000 0000 0000 0001	$-V_{REF}$ (1/65,536)
0000 0000 0000 0000	0V

Figure 1. Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$

APPLICATIONS INFORMATION

4-Quadrant Multiplying Mode ($V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1596-1 can be used with a dual op amp and three external resistors to provide 4-quadrant multiplying operation as shown in Figure 2. With a fixed 10V reference, the circuit shown gives a precision bipolar –10V to 10V output swing.

Op Amp Selection

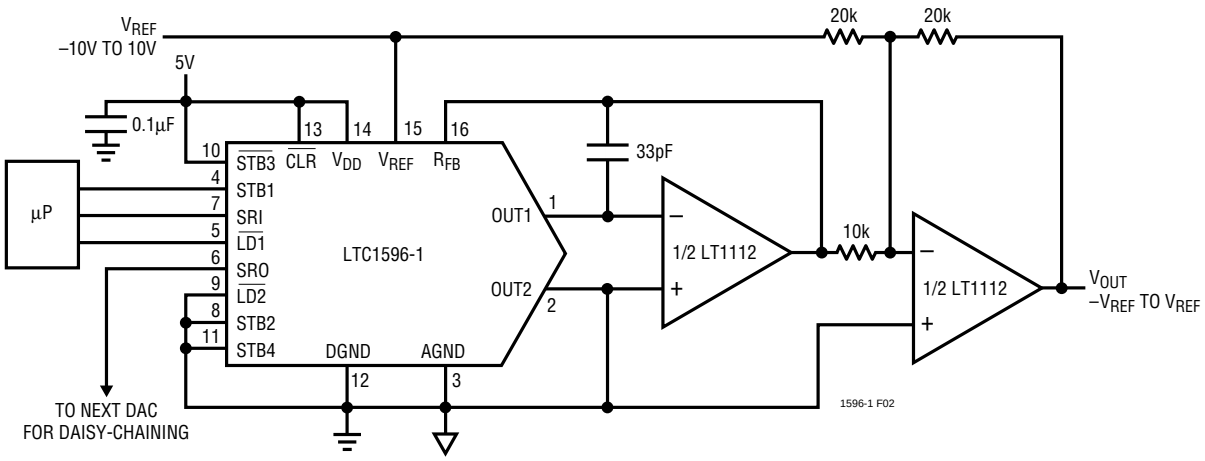
Because of the extremely high accuracy of the 16-bit LTC1596-1, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For example, a 500μV op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error equal to twice the op amp offset. For example, the same 500μV op amp offset will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}) = I_{BIAS}(R_{REF}) = I_{BIAS}(7k)$.

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. I_{OUT2} must be tied to the star ground with as low a resistance as possible.



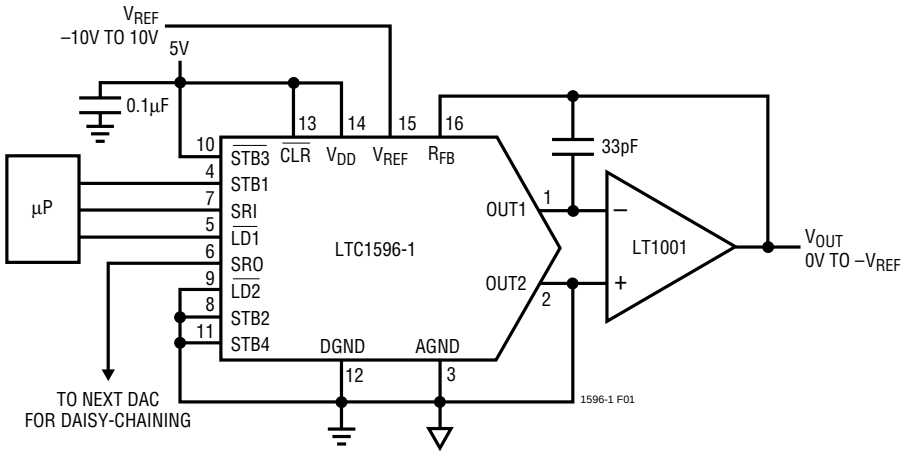
Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT V_{OUT}
MSB LSB	
1111 1111 1111 1111	V_{REF} (32,767/32,768)
1000 0000 0000 0001	V_{REF} (1/32,768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ (1/32,768)
0000 0000 0000 0000	$-V_{REF}$

Figure 2. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

TYPICAL APPLICATION

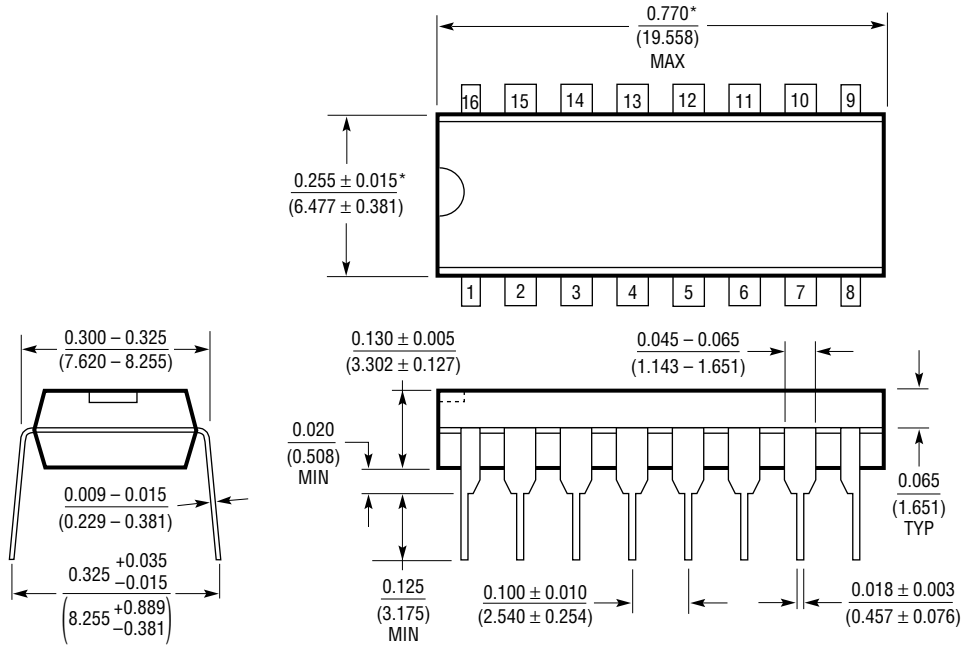
Unipolar Operation (2-Quadrant Multiplication) V_{OUT} = 0V to $-V_{REF}$



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



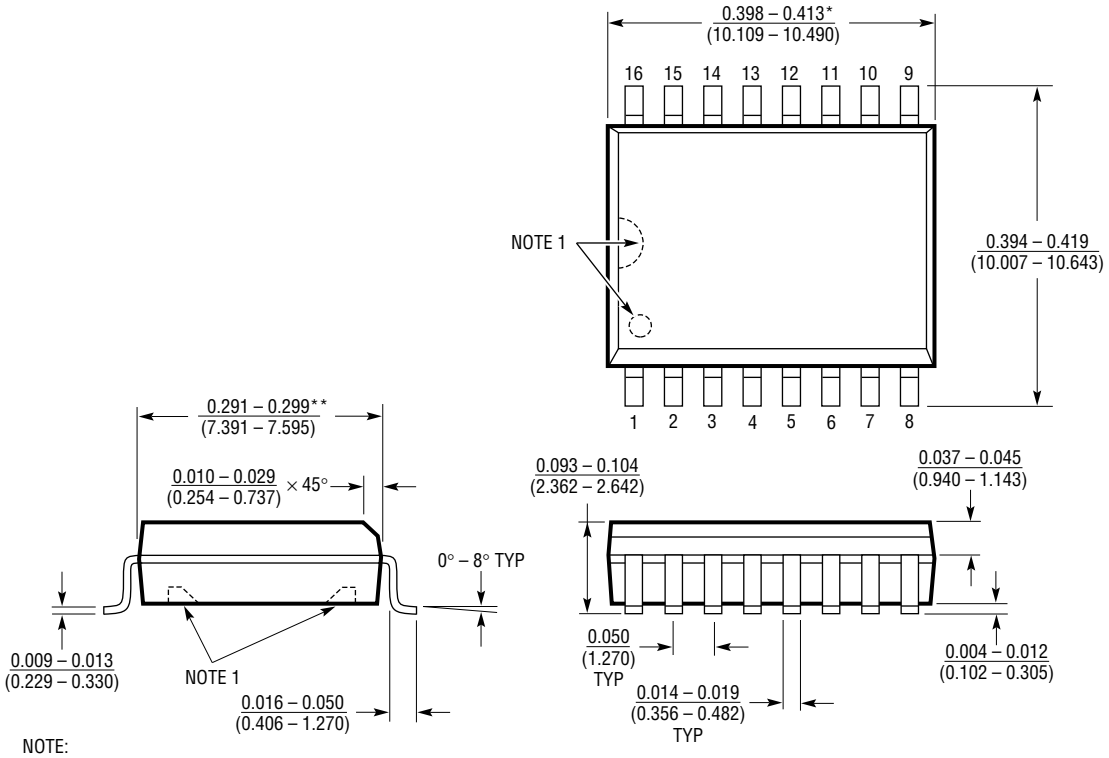
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N16 1197

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
16-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

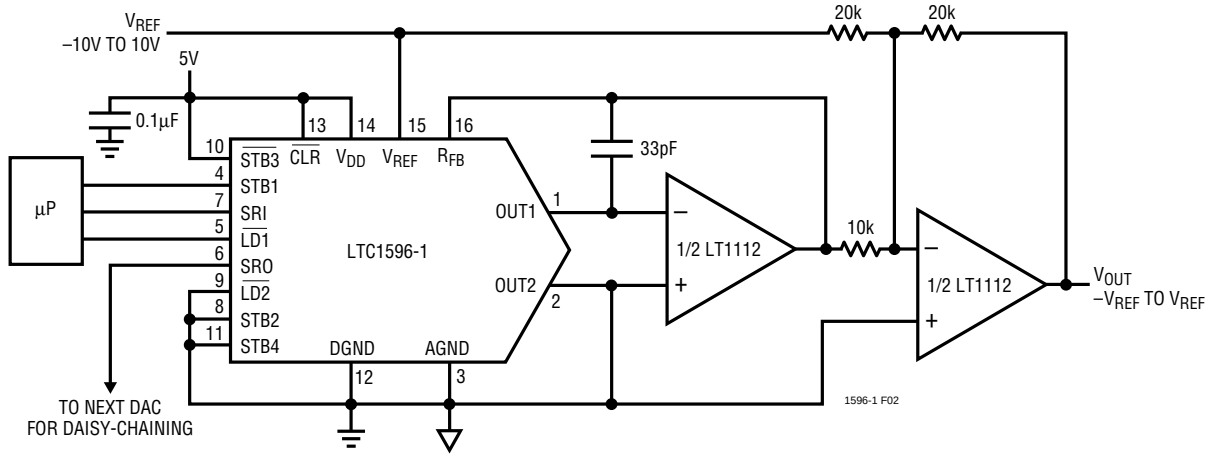
S16 (WIDE) 0396

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1590	Dual Serial I/O Multiplying I_{OUT} 12-Bit DAC	16-Pin SO and PDIP, SPI Interface
LTC1595	16-Bit Mulitplying I_{OUT} DAC in SO-8	True 16-Bit Upgrade for DAC8043
LTC1596	16-Bit Mulitplying I_{OUT} DAC	True 16-Bit Upgrade for DAC8143 and AD7543, Clears to Zero Scale
LTC7541A	Parallel I/O Multiplying I_{OUT} 12-Bit DAC	12-Bit Wide Parallel Input
LTC7543/LTC8143	Serial I/O Multiplying I_{OUT} 12-Bit DACs	Clear Pin and Serial Data Output (LTC8143)
LTC7545A	Parallel I/O Multiplying I_{OUT} 12-Bit DAC	12-Bit Wide Latched Parallel Input
LTC8043	Serial I/O Multiplying I_{OUT} 12-Bit DAC	8-Pin SO and PDIP

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